



Attorney's Docket No.: 10559-305US1/P9626US  
Intel Corporation

*ITM* 2154

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.                      Art Unit: 2154  
Serial No.: 10/069,229                                      Examiner:  
Filed : February 22, 2002  
Assignee : Intel Corporation  
Title : BRANCH INSTRUCTION FOR PROCESSOR ARCHITECTURE

**Mail Stop Amendment**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first Office action on the merits. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

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Examiner's initials in the left column per MPEP 609 are  
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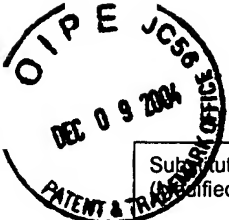
Respectfully submitted,

Date: December 3, 2004

  
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Substitute Form PTO-1449 (Unmodified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-305US1	Application No. 10/069,229
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date February 22, 2002	Group Art Unit 2154

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	09/473,571	12/28/1999	Wolrich et al.			
	AB	09/475,614	12/30/1999	Wolrich at al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AI	WO 01/16697	03/2001	WIPO				
	AJ	WO 01/16698	03/2001	WIPO				
	AK	WO 01/16702	03/2001	WIPO				
	AL	WO 01/16703	03/2001	WIPO				
	AM	WO 01/16713	03/2001	WIPO				
	AN	WO 01/16714	03/2001	WIPO				
	AO	WO 01/16715	03/2001	WIPO				
	AP	WO 01/16722	03/2001	WIPO				
	AQ	WO 01/16758	03/2001	WIPO				
	AR	WO 01/18646	03/2001	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AS	Paver et al., "Register Locking in Asynchronous Processor Computer Design: VLSI Processors," ICCD '92 Proceedings, IEEE 1992 International Conference, 1992, pp. 351-355.
	AT	Waldspurger et al., "Register Relocation: Flexible Contents for Multithreading," Proceedings of the 20th Annual International Symposium on Computer Architecture," 1993, pp. 120-130.
	AU	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	